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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,133	12/01/2003	Chang-Hun Lee	8071-42 (OPP 030497US)	2641

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EXAMINER	
CHEN, WEN YING PATTY	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,133	LEE ET AL.	
	Examiner	Art Unit	
	Wen-Ying P. Chen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *21-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I (claims 1-20) in the reply filed on Feb. 3, 2006 is acknowledged. The traversal is on the ground(s) that although Group I and Group II may be distinct, but the Applicants believe that simultaneous examination will present an undue burden. This is not found persuasive because the two species are patentably distinct from one another such that different effects result due to the different construction of the pixel regions, thus, different search and analysis is required.

The requirement is still deemed proper and is therefore made FINAL.

Response to Amendment

Applicant's Amendment filed Oct. 28, 2005 has been received and entered. With respect to Applicant's election of Species I, claims 21-37 are thus withdrawn from consideration. Therefore, claims 1-20 are now pending in the current application.

Claim Objections

Claims 9 and 10 are objected to because of the following informalities: both claims recites "the first signal line", which should be read as "the first gate line" so as to correspond to claim 1 in which claims 9 and 10 depend upon. Appropriate correction is required.

Claim Rejections - 35 USC § 102

Claims 1-4, 8-11, 14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanagawa et al. (US 2002/0113936).

With respect to claim 1 (Amended): Yanagawa et al. disclose in Figure 5 a liquid crystal display, comprising:

a substrate;

a gate line (element 2) formed on the substrate and extending in a first direction;

a data line (element 3) intersecting the first direction;

a first pixel electrode (element 5) formed in a pixel area defined by intersections of the gate ling and the data line, the first pixel electrode formed substantially parallel to the gate line;

a pixel signal line (elements PSL and Cadd as shown in the figure below) connected to the pixel electrode;

a switching element (element TFT) connected to the gate line, the data line, and the pixel signal line;

a first common electrode (element 4A) formed in the pixel area parallel to the first pixel electrode;

a common signal line (element 4) formed in the pixel area connected to the common electrode;

a first capacitor electrode (element Cadd) formed in the pixel area connected to the pixel signal line;

a second capacitor electrode (element 4, the portion overlapping Cadd) formed in the pixel area connected to the common signal line;

a second pixel electrode (element 5) formed in the pixel area opposite to the first pixel electrode and connected to the pixel signal line; and

a second common electrode (element 4A) formed in the pixel area, the second common electrode opposite to the first common electrode and connected to the common signal line.

As to claim 2: Yanagawa et al. further disclose in Figure 5 that the pixel signal line (element PSL as shown in the figure below) overlaps the common signal line (element 4).

As to claim 3: Yanagawa et al. further disclose in Figure 5 that the common signal line (element 4, the portion connecting all the common electrodes) is parallel to the data line (element 3).

As to claim 4 (Amended): Yanagawa et al. further disclose in Figure 5 that the distance between the common signal line (element 4, the portion connecting all the common electrodes adjacent to the data line) and the data line (element 3, not shown but to the right of the pixel) is shorter than the distance between the pixel signal line (element Cadd, which is also part of element PSL) and the switching element (element TFT).

As to claim 8: Yanagawa et al. further disclose in Figure 5 that the second capacitor electrode (element 4, portion corresponding to Cadd) is triangular in shape.

As to claim 9: Yanagawa et al. further disclose in Figure 5 that the first common electrode (element 4A) is disposed nearer to the gate line (element 2) than the first pixel electrode (element 5).

As to claim 10: Yanagawa et al. further disclose in Figure 5 that the second common electrode (element 4A) is disposed nearer to the gate line (element 2) than the second pixel electrode (element 5).

As to claim 11 (Amended): Yanagawa et al. further disclose in Figure 5 and Paragraph 0047 that the liquid crystal display further comprises a plurality of pixel areas disposed along the direction of the gate line (wherein the pixel areas are formed in a matrix).

As to claim 14: Yanagawa et al. further disclose in Paragraph 0049 that the pixel electrode and the common electrode are disposed on the same planar plane.

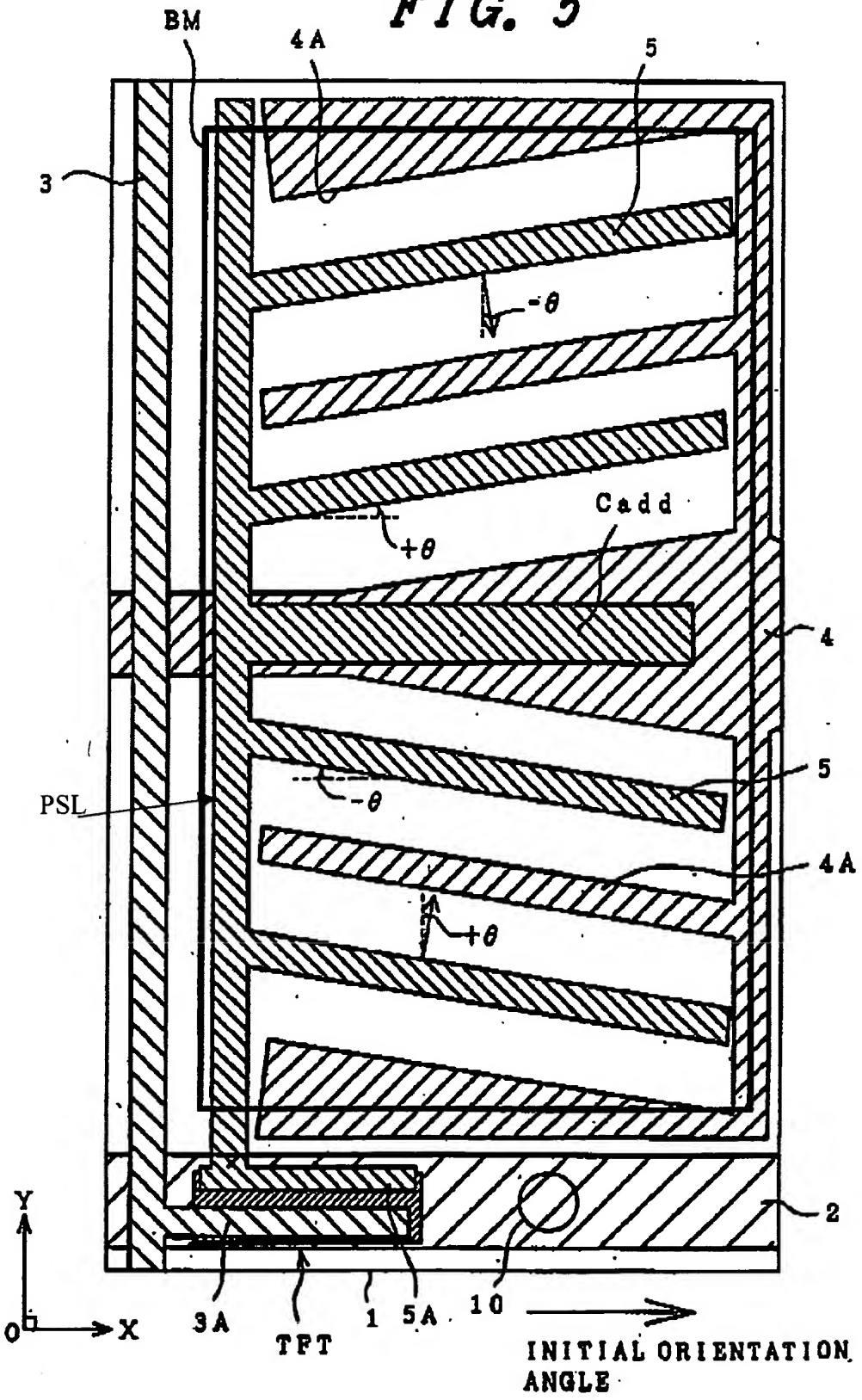
As to claim 16: Yanagawa et al. further disclose in Figure 5 that the capacitor electrodes (element Cadd and 4) are disposed in a longitudinal center of the pixel area.

As to claim 17: Yanagawa et al. further disclose in Figure 5 that the first capacitor electrode (element Cadd) is a part of the first pixel electrode (element 5).

As to claim 18: Yanagawa et al. further disclose in Figure 5 that the pixel area has a rectangular shape.

As to claim 19: Yanagawa et al. further disclose in Paragraph 0047 that the gate line is formed of at least one material selected from a group of Al, Al-alloy, Ag, Ag-alloy and its alloy.

FIG. 5


BM
4A
5
3
-θ
Cadd
+θ
4
PSL
5
-θ
4A
+θ
Y
2
0
X
3A
TFT
1
5A
10
INITIAL ORIENTATION ANGLE

Claim Rejections - 35 USC § 103

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa et al. (US 2002/0113936) in view of Wang et al. (US 6201273).

Yanagawa et al. disclose all of the limitations set forth in claim 1 and further disclose in Figure 5 that the second capacitor electrode (element 4, portion corresponding to Cadd) is triangular in shape, but fail to disclose that the first capacitor electrode is triangular in shape.

However, Wang et al. disclose in Column 7, lines 35-39 that the capacitors can be formed in shapes such as rectangular, square, and triangular depending on the application.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display comprising the substrate structure as taught by Yanagawa et al. wherein the first capacitor electrode is in a triangular shape as taught by Wang et al. so as to correspond to the triangular shape of the second capacitor electrode disclosed by Yanagawa et al., such that with matching surface area of the capacitor electrodes, the capacitance can thus be maximized.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa et al. (US 2002/0113936) in view of Song et al. (US 2001/0040647).

Yanagawa et al. disclose all of the limitations set forth in the previous claims, but fail to disclose that the pixel electrode and the common electrode have a thickness of less than about 2000 Å.

However, Song et al. disclose in Paragraph 0037 that the pixel electrode and the common electrode are formed to have a thickness of 500 Å, which is less than 2000 Å.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display comprising the substrate structure as taught by Yanagawa et al. wherein the pixel electrode and the common electrode are formed to have a thickness of 500 Å as taught by Song et al., since Song et al. teach that such thickness of the electrodes helps to maintain a flat surface so as to result in a uniform rubbing and thus the light leakage may be reduced (Paragraph 0037).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa et al. (US 2002/0113936) in view of Moon et al. (US 2002/0044246).

Yanagawa et al. disclose all of the limitations set forth in claim 19, but fail to specifically disclose that the first signal line further comprises a pad layer.

However, Moon et al. disclose in Figure 6 a liquid crystal display device wherein the gate line (element 132) comprises of a pad layer (element 126).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display comprising the substrate structure as taught by Yanagawa et al. wherein the gate line further comprises of a pad layer as taught by Moon et al., since Moon et al. teach that the pad layer is formed so that a gate voltage from the exterior to the TFT array can be applied to the gate lines (Paragraph 0036).

Claims 1, 5-6 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota (US 2002/0044249) in view of Yanagawa et al. (US 2002/0113936).

With respect to claim 1 (Amended): Hirota discloses in Figure 5 a liquid crystal display, comprising:

a substrate;

a gate line (element 1) formed on the substrate and extending in a first direction;

a data line (element 2) intersecting the first direction;

a first pixel electrode (element 5) formed in a pixel area defined by intersections of the gate ling and the data line, the first pixel electrode formed substantially parallel to the gate line;

a pixel signal line (elements PSL as shown in the figure below) connected to the pixel electrode;

a switching element (element 4) connected to the gate line, the data line, and the pixel signal line;

a first common electrode (element 6) formed in the pixel area parallel to the first pixel electrode;

a common signal line (element 3) formed in the pixel area connected to the common electrode;

a second pixel electrode (element 5) formed in the pixel area opposite to the first pixel electrode and connected to the pixel signal line; and

a second common electrode (element 6) formed in the pixel area, the second common electrode opposite to the first common electrode and connected to the common signal line.

Hirota fails to disclose the formation of capacitor electrodes.

However, Yanagawa et al. disclose in Figure 5 and Paragraph 0054 forming capacitor electrodes in the pixel area such that a first capacitor electrode (element Cadd) is formed in the pixel area connected to the pixel signal line and a second capacitor electrode (element 4, the portion overlapping Cadd) formed in the pixel area connected to the common signal line.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display as taught by Hirota wherein the pixel area further comprises of capacitor electrodes as taught by Yanagawa et al., since Yanagawa et al. teach that by forming capacitor electrodes in the pixel area helps to improve the data retentivity (Paragraph 0054).

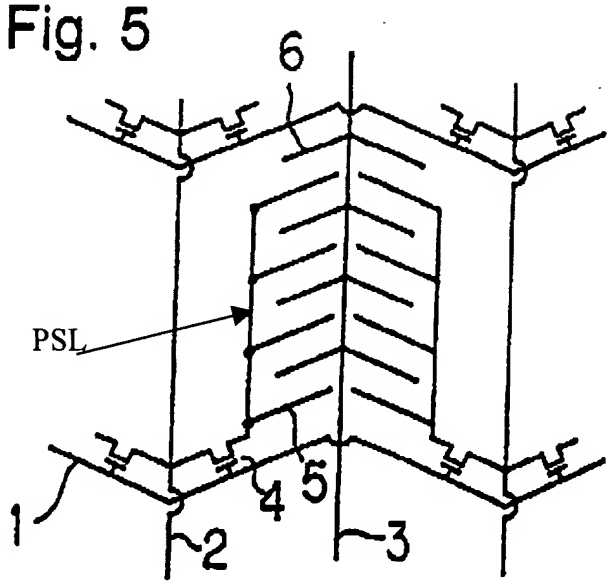
As to claim 5 (Amended): Hirota further disclose in Figure 5 that the gate line (element 1) bends at a positive or negative angle with respect to the perpendicular direction of the data line (element 2).

As to claim 6 (Amended): Hirota further disclose in Paragraph 0046 that the gate line is bent at a positive or negative angle with respect to the direction of a rubbing direction on the substrate.

As to claim 11 (Amended): Hirota further disclose in Figure 5 that the display further comprises a plurality of pixel areas disposed along the direction of the gate line (element 1).

As to claim 12(Amended): Hirota further disclose in Figure 5 that the display further comprises a plurality of pixel areas disposed symmetrically with respect to the data line (element 2) therebetween.

Fig. 5



Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirota (US 2002/0044249) and Yanagawa et al. (US 2002/0113936) in view of Moia (US 6806930).

Hirota and Yanagawa et al. disclose all of the limitations set forth in the previous claims, but fail to disclose that the pixel area is triangular in shape.

However, Moia teaches in Column 9, lines 31-37 that the shape of the pixel area can be of rhombic, triangle, hexagonal, or randomly organized arrangements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct a liquid crystal display comprising the substrate structure as taught by Hirota and Yanagawa et al. wherein the pixel are is in the shape of a triangle as taught by Moia so that the irregularity of the pixel shape helps to achieve wider viewing angle of the liquid crystal display.

Response to Arguments

Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wen-Ying P. Chen whose telephone number is (571)272-8444. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wen-Ying P Chen
Examiner
Art Unit 2871

WPC
3/10/06

ANDREW SCHECHTER
PRIMARY EXAMINER